UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/800,145	03/06/2001	Paul W. Dent	4015-815	4516

24112 7590 05/27/2005

COATS & BENNETT, PLLC
P O BOX 5
RALEIGH, NC 27602

EXAMINER	
KLIMACH, PAULA W	

ART UNIT	PAPER NUMBER
2135	

DATE MAILED: 05/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/800,145	DENT ET AL.	
	Examiner	Art Unit	
	Paula W. Klimach	2135	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

S.O.O.

DETAILED ACTION

Response to Amendment

This office action is in response to amendment filed on 02/24/05. The amendment filed on 02/24/05 have been entered and made of record. Therefore, presently pending claims are 1-42.

Response to Arguments

Applicant's arguments filed 02/04/05 have been fully considered but they are not persuasive because of following reasons. The examiner expresses regret for having failed to address the claims 27-42 in the previous office action. The office current action is a non-final as promised.

Applicant argued none of the references teach or suggest the interoperation between the host processor and the coprocessor. This is not found persuasive. Although it is true that none of the reference teach this feature alone (as that would have resulted in a 102 rejection) the combination of the references White, Heikes, and Wey disclose the interrelationship between the coprocessor and the processor. By the fact that the system of White discloses a processor and Heikes and Wey disclose coprocessors, which by virtue of there being coprocessor inter relate with a processor. In the combination of White, Heikes, and Wey the coprocessors of Heikes and Wey are introduced to interrelate with the processor of White.

The applicant argues further that White fails to teach or suggest both the host processor and the co-processor (both of which operate recursively to reduce their respective staring values). The applicant also argues that it means that White fails to teach or suggest that the host processor provides recursively reduced length integer values to the co-processor (for further recursive

reduction). Although it is true that White does not disclose a coprocessor, as stated above, the combination of White, Heikes, and Wey disclose, in the previous office action, the co-processor wherein the processor disclosed by White divides the input into groups which then need to be multiplied by the coprocessor of Keikes and Wey introduced in the afore mentioned combination.

The applicant argues further that Heikes discloses nothing regarding recursive operations. This is not found persuasive because in the combination of White, Heikes, and Wey, Wey discloses a multiplier designed to recursively decompose and then execute the time consuming multiplication process (abstract).

The applicant also argues that Wey does not identify the disclosed circuit as a co-processor. However a multiplier is a co-processor. The applicant argues further that the values partitioned by the multiplier of Wey are not reduced length integer values produced recursivel by a host processor. As disclosed above the combination of White, Heikes, and Wey, the reference of White discloses the processor that reduces the length of the integer values.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the references are used to improve multiplication and therefore the special case of squaring.

The examiner asserts that White, Heikes, and Wey do teach or suggest the subject matter broadly recited in independent Claims 1, 9, 17. Dependent Claims 2-8, 10-16, and 18-26 are also rejected at least by virtue of their dependency on independent claims and by other reason set forth in this office action. Accordingly, rejections for claims 1-26 are respectfully maintained.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over White in view of Wey and Heikes et al.

In reference to claim 17 White discloses a system and method for computing the square of a value (abstract). The method of White comprising a processor to compute the square of a long integer where in the processor reduces the integer values into a most significant part and a least significant part and sending it to a multiplier (Fig. 1 and Fig. 2). Thus the starting value is reduced.

Although White discloses a processor that reduces the integer value to half of the length of the starting integer; and a square is a special case of multiplication, White does not expressly disclose a co-processor connected to said host processor; and the host processor disclosed by White does not compute the square of a long integer value by recursively reducing said square of

said long integer value into a combination of squares of reduced integer values, wherein at each step of said recursion said host processor reduces starting integer values to a combination of squares of three ending integer values of one-half the length of said starting integer values, and wherein at each step of said recursion said host processor randomly orders said ending integer values; and

Heikes discloses a multiplier, coprocessor, as a part of a processor and therefore connected to the host processor (paragraph 1 page 290). The coprocessor is a processor that specializes in multiplication.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use a multiplier for multiplication in a chip as in Heikes in the system of White. One of ordinary skill in the art would have been motivated to do this because a coprocessor is a specialized processor that is produced to increase the speed of the operation, thus the multiplier would increase the speed at which multiplication and therefore squaring is performed.

Wey discloses a multiplier, coprocessor, designed to recursively decompose and then execute the time consuming multiplication process (abstract). The system disclosed by Wey discloses recursively reducing the input to a combination of multiplications, squares, of half the length of the starting values (page 329 paragraph 2). Then finally the hardware logic ciruits perform the multiplication, square of the hardware length integer values (Fig. 9).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use a coprocessor that computes the multiplication recursively as in the system for Wey for the reduced starting values as in the system by White. One of ordinary skill in the art would have been motivated to do this because it would gain a significant performance

increase.

In reference to claims 1, 9, 18, and 29 White discloses a system and method for computing the square of a value (abstract). The method of White comprising a processor to compute the square of a long integer where in the processor reduces the integer values into a most significant part and a least significant part and sending it to a multiplier (Fig. 1 and Fig. 2). Thus reducing the starting values

Although White discloses a processor that reduces the integer value to half of the length of the starting integer; and a square is a special case of multiplication, White does not expressly disclose a co-processor connected to said host processor to compute the squares of said reduced length integer values by further recursively reducing the squares of said reduced integer values into a combination of squares of hardware-length integer values that can be squared by hardware logic circuits, wherein at each step of said recursion said co-processor reduces starting integer values to a combination of squares of three ending integer values of one-half the length of said standing integer values; and one or more hardware logic circuits to square said hardware-length integer values.

Heikes discloses a multiplier, coprocessor, as a part of a processor and therefore connected to the host processor (paragraph 1 page 290).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use a multiplier, coprocessor, in a chip for multiplication as in Heikes in the system of White. One of ordinary skill in the art would have been motivated to do this because a coprocessor is a specialized processor that is produced to increase the speed of the operation, thus the multiplier would increase the speed at which multiplication and therefore squaring is

performed.

Wey discloses a multiplier, coprocessor, designed to recursively decompose and then execute the time-consuming multiplication process (abstract). The system disclosed by Wey discloses recursively reducing the input to a combination of multiplications, squares, of half the length of the starting values (page 329 paragraph 2). Then finally the hardware logic circuits perform the multiplication, square of the hardware length integer values (Fig. 9).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use a coprocessor that performs recursive multiplications as in Wey in the system of White. One of ordinary skill in the art would have been motivated to do this because it would gain a significant performance increase.

In reference to claims 27, 31, 33, and 39, a square is a special case of multiplication wherein the two values being multiplied are equal. Claim 27 is therefore rejected as in claim 1, noting that the applicant disclosed the similarity in amendment of 02/24/05.

In reference to claims 2, 10, 19-20, and 35, wherein said one or more hardware logic circuits comprise a separate hardware logic circuit for each hardware-length integer value to be squared (Fig. 6 of Wey).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use a coprocessor that performs recursive multiplications as in Wey in the system of White. One of ordinary skill in the art would have been motivated to do this because it would gain a significant performance increase.

In reference to claims 3, 11, 21, and 34, 40 wherein said host processor further computes the product of two long integer values by computing the difference between the square of the

sum of said two long integer values and the square of the difference of said two long integer values (Fig. 2).

In reference to claims 4, 12 and 22 wherein said host processor divides said sum of said two long integer values and said difference of said two long integer values by two before computing said squares of said sum and said difference (Fig 2).

In reference to claims 5, 13, 23, and 36-37 wherein said host processor adds the smaller value of said two long integer values to the difference of said squares to form said final product (Fig. 2).

In reference to claims 6, 14, 24, and 41 wherein said host processor further computes a power of a long integer value by computing successive squares of said long integer value and by computing the product of selected ones of said successive squares corresponding to binary "1"s in said power (column 7 lines 60-68).

In reference to claims 7, 15, 25, and 42 wherein said host processor computes said product of selected ones of said successive squares by computing the difference between the squares of the sum and the difference of said successive squares (column 5 lines 24-35).

In reference to claims 8, 16, 26, 30, 28, and 32 further comprising randomly ordering each set of three ending integer values in at least one stage of said recursion (page 331 part 3.2).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to shuffle the set of inputs as in Wey in the system of White. One of ordinary skill in the art would have been motivated to do this because it would gain a significant performance increase.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paula W. Klimach whose telephone number is (571) 272-3854. The examiner can normally be reached on Mon to Thr 9:30 a.m to 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Vu can be reached on (571) 272-3859. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PWK
Monday, May 23, 2005

KIM VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100